Gate Workfunction Optimization of a 32 nm Metal Gate MOSFET for Low Power Applications

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Abstract - The feasibility of a midgap metal gate is investigated for a 32 nm MOSFET for low power applications. The midgap metal gate MOSFET is found to deliver \( I_{on} \) as high as a bandaged gate if a proper retrograde channel is used. An adequate design of the retrograde channel is essential to achieve the performance requirement given in the ITRS roadmap. A process simulation is also run to evaluate the feasibility of the necessary retrograde profile in manufacturing environments. Based on the simulated result, it is found that any subsequent thermal process should be tightly controlled to retain transistor performance, which is achieved using the retrograde doping profile. Also, the bandaged gate MOSFET is determined to be more vulnerable to the subsequent thermal processes than the midgap gate MOSFET. A guideline for workfunction (\( \Phi_m \)) is suggested for the 32 nm MOSFET.

Keywords: gate workfunction (\( \Phi_m \)), low power, metal gate, retrograde channel, \( V_t \) roll-off

1. Introduction

A metal gate has been suggested for 32 nm CMOS technology to eliminate the adverse effects of poly depletion, boron penetration and high poly sheet resistance [1]. In selecting the gate metal material, the workfunction of the metal gate should be given the most consideration since it determines the threshold voltage (\( V_t \)) of the MOSFET. A bandaged metal gate was previously reported to be the optimal choice for sub-50 nm high performance applications (about 4.2 eV for NMOS and 5.1 eV for PMOS) [2],[3]. However, when CMOSFET is integrated, use of the bandaged metal gate makes the fabrication process complicated and expensive. To improve the manufacturability of the bandaged metal gate MOSFET, various schemes have been reported [4], but yet being able to offer a simple solution. In this work, we investigate the feasibility of a midgap gate for low power application, where relatively high \( V_t \) is required. The device performance of a midgap metal gate MOSFET is compared against that of a bandaged metal gate using TCAD simulation. In addition, the feasibility of the necessary channel doping profile required for different gate workfunctions is studied at various thermal budgets.

2. Simulation Methodology

A commercial device and process simulator ATLAS/ATHENA from SILVACO have been used for this work. Classical drift and diffusion model have been used. For carrier mobility, field and concentration dependent models have been used. The equivalent oxide thickness of the gate dielectric is 1.5 nm. It is assumed that junction depth of S/D extension and S/D are 8.8 nm and 18 nm, respectively. Also, the doping concentration of S/D and S/D extension are assumed to be \( 2.0 \times 10^{20} \text{ cm}^{-3} \) and \( 8.0 \times 10^{19} \text{ cm}^{-3} \), obtained from ITRS [1]. The nominal gate length is 32 nm and \( \pm 4 \text{ nm gate CD variation is considered (identified as L}_\text{s}, \text{ L}_\text{nom}, \text{ L}_\text{o} \text{, respectively). Supply voltage of 1.1V is used. Additional conditions will be followed in the next section.}

3. Results and Discussion

To meet \( I_{on} = 300 \text{ pA/\mu m at L} \text{ devices, substrate doping concentrations are calculated for various gate workfunctions in Fig. 1. A retrograde channel and a uniform channel are considered. The retrograde channel consists of a 5 nm-deep lightly doped (1.0 \times 10^{16} \text{ cm}^{-2}) \) region under which the highly doped substrate lies. For MOSFET performance comparison, \( I_{on} \) at \( L_s \) and \( L \) are calculated as indicated in Fig. 2. It is shown that use of the retrograde channel enables the improvement of \( I_{on} \) for midgap gate MOSFET by taking advantage of high mobility and suppressing short channel effect (SCE).

Note that the retrograde channel provides higher \( I_{on} \) than

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Received October 14, 2005 ; Accepted November 26, 2005
the uniform channel for both NMOS and PMOS.

![Graph showing substrate doping concentration vs gate workfunction for NMOS and PMOS with square and circle symbols]

**Fig. 1** Substrate doping concentration required to meet a given $I_{off}$ for L. devices

$I_{on}$ of the midgap ($\Phi_m = 4.7$ eV for both NMOS and PMOS) gate device with the retrograde channel is comparable to that of the optimum workfunction device with the uniform channel ($\Phi_m = 4.4$ eV for NMOS, $\Phi_m = 4.9$ eV for PMOS).

In SiO$_2$ based gate dielectric transistors, a steep retrograde channel has been known to be impractical due to the high temperature gate oxidation process and S/D activation process. However, for 32 nm CMOS technology, the use of alternative gate dielectric materials such as HfO$_2$ is very likely expected and enables the preservation of the implanted retrograde channel even after the gate dielectric formation because of its low temperature process [5]-[7]. The following thermal processes such as RTA, spike annealing for S/D activation and low temperature side wall process [8],[9] are expected to diffuse dopants insignificantly. Considering the usable processes and heavy implanted species, such as indium (In) the necessary retrograde channel will be likely obtained for 32 nm CMOS technology.

To investigate the feasibility of the necessary retrograde channel, a process simulation has been performed. Indium (In) and arsenic (As) were used for the retrograde channel and the S/D implants, respectively. Presented in **Fig. 3** is the substrate implant dose, required to meet given $I_{off}$ at L. devices with various annealing time and gate workfunction. An identical S/D is assumed for the various conditions.

![Graph showing indium implant dose vs anneal time for different workfunctions]

**Fig. 3** Required indium implant dose to meet $I_{off} = 300$ pA/µm for L. device with annealing at 1000°C

As anneal time increases, the required implant dose increases in order to suppress lateral diffusion of S/D, more evident in the midgap gate device. Using the implant condition in **Fig. 3**, $I_{on}$ is calculated as the anneal time increases (**Fig. 4**). It is observed that $I_{on}$ degrades dramatically as the anneal time increases because the retrograde channel profile can not be maintained in the longer anneal.

![Graph showing $I_{on}$ vs workfunction for different implant energies and anneal times]

**Fig. 2** Comparison of $I_{on}$ of NMOS (a) and PMOS (b) Both a uniform and a retrograde channel are used.
Fig. 4 Degradation of $I_{on}$ caused by subsequent thermal processes. $I_{on}$ represents $I_{on}$ of L device without anneal.

The annealing process results in a high surface doping concentration and consequently it causes lower carrier mobility. Fig. 4 indicates that the bandedge gate device degrades more than the midgap gate devices, suggesting the resulting channel profile be further deviated from the one calculated in Fig. 1. However, the lesser degradation of the midgap gate device is not observed in the L+ device as indicated in Fig. 4. To understand the phenomenon, $V_t$ roll-off is studied as the anneal increases.

Fig. 5 $V_t$ roll-off as a function of anneal time. $\Delta V_t$ is obtained using $V_t (L_-) - V_t (L_+)$

Fig. 6 illustrates the schematic channel doping profile obtained using halo or uniform channel implants. The derived equation (1) predicts that a shorter effective channel (shorter $L_{eff}$) would experience more changes in the effective channel doping ($\Delta N_A^{eff}$) for the given gate CD variation ($\pm 15\%$).

$$N_A^{eff} (L_{eff}) = N_A^{mid} \frac{L_2}{L_1 + 2L_2}$$

(+: with halo, -: w/o halo)

where $L_{eff} = L_1 + 2L_2$

$$\Delta N_A^{eff} = N_A^{eff} (L_{eff}) - N_A^{mid} (L_{eff} + \Delta L)$$

$$= \pm \frac{N_A^{mid} L_2}{(L_1 + 2L_2)} \left[ \frac{1}{\Delta L} \right]$$

$$\left[ \frac{1}{\Delta L} \right]$$

(1)

Thus, in the shorter effective channel length, resulted from the longer anneal, the more severe $V_t$ roll-off should be expected for the given gate CD variation. This model implies that the midgap gate device, in which the large lateral S/D diffusion is observed, is expected to suffer from the more severe $V_t$ roll-off.

4. Conclusion

The midgap metal gate device is found to deliver high $I_{on}$ when a proper retrograde channel is used. However, the performance can be rapidly diminished unless the subsequent thermal process is tightly controlled, especially in the case of the bandedge gate device. In addition, the analytic effective channel doping model predicts the midgap gate device will experience more severe $V_t$ roll-off than the bandedge device due to shorter $L_{eff}$. Based on the simulated results, 4.4 eV (nMOS) and 4.9 eV (pMOS) gate
workfunctions are found to be optimum for the low power applications.

Acknowledgements

This work was supported by the "System IC 2010" project of the Korea Ministry of Science and Technology and the Ministry of Commerce, Industry and Energy.

References


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